dV/dt EFFECTS IN MOSFET AND BIPOLAR JUNCTION TRANSISTOR SWITCHES

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ABSTRACT

Spurious turn-on due to dV/dt triggering is a real possibility in high speed switching circuits using MOSFETs or bipolar junction transistors (BJTs). This paper discusses the mechanisms leading to spurious turn-on, test methods to determine dV/dt limits, the effect of dV/dt turn-on circuit operation, and methods to minimize dV/dt triggering in practical circuits.

INTRODUCTION

Most designers of power switching circuits are well aware of the dV/dt limitations of SCRs which, if exceeded, can cause these devices to turn on in the absence of a normal trigger pulse. Despite an earlier discussion of the problem (1) it is not generally appreciated that a similar, and equally detrimental phenomenon, can appear in both BJTs and MOSFETs. Until the last few years very few BJTs were available which could switch fast enough to induce false triggering in most circuits. In the special case of a resonant circuit being driven off resonance, it was possible to see dV/dt triggering with even relatively slow switching times but very few designers ever encountered this application so that dV/dt triggering remained a matter of academic rather than practical interest. In the last three to four years however, BJTs have shown dramatic improvements in switching times. It is now readily possible to obtain 450V devices that can turn on in 50-70 nsec. In addition, the power MOSFET has become a practical reality and a 450V MOSFET can be switched on in 4-5 nsec generating transitions exceeding 100V/nsec.

Off line converters operating with switching frequencies well above 100kHz are becoming very common. For a variety of practical reasons resonant converter topologies are frequently used in high frequency regulators. Many designers who formerly used only switchmode circuits are increasingly turning to resonant circuits.

Because of these device changes and the changes in circuit practice, spurious turn-on due to false triggering is no longer an academic possibility, it has become a practical problem. The following discussion is intended to illuminate the mechanisms causing the problem, to show test circuits determining the dV/dt capability of a device and to present some methods to circumvent or eliminate the problem.

MECHANISMS RESPONSIBLE FOR SPURIOUS TURN-ON

Neither the MOSFET nor the BJT is a perfect switch. Both devices have parasitic capacitances at the input and from input to output. In addition any practical drive circuit will have some residual resistance when the switch is off.

Equivalent circuits for the MOSFET and BJT taking into account these parasitic elements are shown in Figure 1. If a positive going voltage ramp is

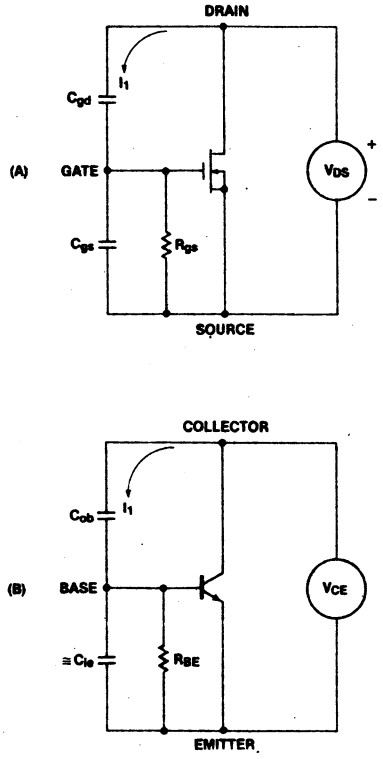

Figure 1

applied either drain-to-source or collector-to emitter a current, I_1, will flow through the feedback capacity (C_{gd} or C_{ob}). If I_1 is sufficiently large the voltage at the gate or base will exceed the turn-on threshold and the switch will turn on, even though the switch is nominally in the off state.

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The important question is: does V_{gs} or V_{BE} exceed the device turn-on threshold or not? To answer this question the equivalent circuit in Figure 2 can be used.

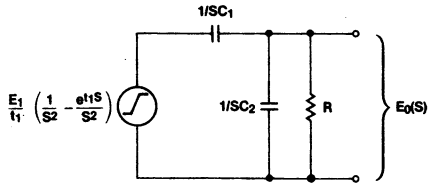

Figure 2

As is shown in appendix 1 the output voltage of the network is:

$$e_o(t)=\frac{\left(\frac{E_1}{t_1}\right)(RC_1)\left(e^{-t/R(C_1+C_2)}\right)\left(e^{t_1/R(C_1+C_2)}\right)}{\left(t_1\right)} \quad (1)$$

The waveform corresponding to this equation is shown in Figure 3.

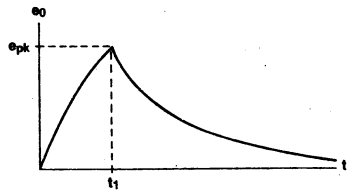

Figure 3

The waveform in Figure 3 applies to V_{GS} for a MOSFET whether below or above $V_{GS(th)}$ presuming that the drain impedance is zero or some small value. Obviously the waveform does not apply when the threshold voltage of the BJT base-emitter diode is exceeded. In that case the waveform would be clamped by the diode. This distinction is really of no great importance. What is important is whether or not e_{pk} is greater than the threshold voltage of the device. The expression for e_{pk} is:

$$e_{pk}=\left(\frac{dV}{dt}\right)(\tau_1)\left(1-e^{-\frac{E_1}{dV/dt}}\right)\left(\frac{1}{\tau_2}\right) \quad (2)$$

where: $\tau_1 = RC_1$

$\tau_2 = R(C_1 + C_2)$

The exponential term of equation 2 is usually quite small so for practical purposes equation 2 may be reduced to:

$$e_{pk} \cong \left(\frac{dV}{dt}\right) RC_1 \quad (3)$$

For a MOSFET where C_1 = 10pF, V_{th} = 3.5V and dV/dt = 50V/ns, the maximum gate to source resistance permissible to avoid false triggering is:

$$R_{gs} \leq \frac{V_{GS(th)}}{(dV/dt)(C_1)} \quad (4)$$

$$R_{GS} \leq 7\Omega$$

The internal gate resistance for such a device could well be as high as 1 to 2Ω. This means that the external resistance due to the drive circuit may need to be less than 5Ω. Strictly speaking this too is an approximation since the internal capacitance and gate resistance form a distributed network more complex than the simple RC network in Figure 2, but the point of this example is that the impedance of the driver must be quite low when the switch is in the off state and some allowance for the internal gate resistance is required.

COMPONENT VALUES

In order to perform the foregoing calculations it is necessary to know the values for C_1, C_2 and V_{th}. For a MOSFET $C_1=C_{gd}$ and $C_2=C_{gs}$. As shown in Figure 4, C_{gs} changes little with variations in V_{DS}. In a BJT C_{ob} will also show a similar strong dependence on V_{CE}. If the calculation is to be performed then the designer must have a curve similar to that shown in Figure 4. If this information is not provided in the data sheet then the test procedure and circuits outlined in appendix 2 can be used to generate the necessary data.

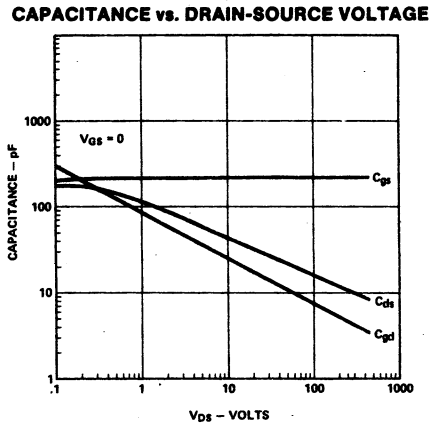

Figure 4

For a silicon BJT $V_{th} \cong .7V$ with a temperature coefficient of about -2 mV/°C. In a MOSFET, V_{th} can have a wide range of values ranging from 1.5 to 7 volts depending on the design of the device. The range of values for V_{th} are usually given in the data sheet but if a more exact value is required V_{th} may easily be measured on a transistor curve tracer. The wise designer will use the worst case low value for V_{th} as given in the data sheet rather than rely on measurements of a few devices which may or may not be typical. The temperature coefficient of V_{th} for the MOSFET can have a wide range of variance, -4 to -8 mV/°C is typical of present power MOSFETS.

Note that for both types of devices the threshold decreases as the temperature increases. At high temperatures the dV/dt capability will be reduced. Another temperature effect is the increase in internal gate resistance, R_G, with temperature in a MOSFET. For a silicon gate device the temperature coefficient is typically .7%/°C. If R_G is a significant portion of the total gate to source impedance then the dV/dt capability will again be decreased at elevated temperatures.

When a BJT is triggered on the time of conduction will be extended by the storage time. Since it is unlikely that during dV/dt triggering the device will be turned on hard enough to allow V_{CE} to fall below V_{BE}, the storage time will be relatively brief. The storage time is a strong function of temperature and at high junction temperatures the conduction time may well be increased significantly.

EFFECT OF REVERSE CURRENT CONDUCTION

Up to this point we have been discussing a model which presumes that immediately before a positive dV/dt is applied that the device is in the quiescent state with at least a small positive potential from drain-to-source or collector-to-emitter. Under these conditions C_1 will be small because the junction with which C_1 is associated will be reversed biased. This assumption is <u>not</u> always valid however.

In a resonant converter or a switching circuit with a reactive load it is possible for the switch to experience reverse current conduction as a normal part of the operating sequence. As shown in Figure 5, it is common practice to connect a diode (D_1) across the switch to carry the reverse load current, I_{LR}. While most of I_{LR} (I_1) will pass through D_1, a small portion (I_2) will flow through the base-collector junction. This junction is now forward biased and the effective value for C_1 can be 100 times larger. If reverse conduction is present immediately before a positive collector-emitter transition then spurious triggering will occur at a much lower value for dV/dt.

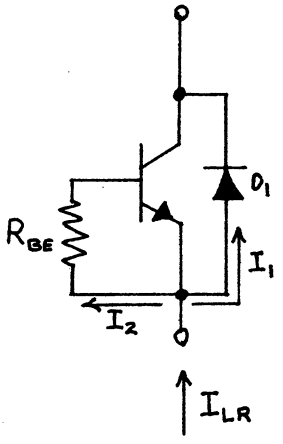

Figure 5

If this is a normal part of the circuit operation then it may be necessary to prevent reverse conduction entirely by using a series diode in the collector. It can be very frustrating to measure the value for C_1, when this junction is in forward conduction, with any accuracy. This is particularly so if the value for I_2 is not determined. A more practical approach would be to use the test circuit, shown later in this paper, with appropriate values for the drive impedance and dV/dt to see if there will be a problem.

THE PARASITIC BJT IN THE MOSFET

Inherent in all present power MOSFET structures there is a parasitic BJT. The presence of this BJT can be seen from Figure 6 which shows the structure of a typical vertical D-MOS device. The N^- epi region corresponds to collector of the BJT. The p diffusion corresponds to the base of the BJT and the N+ diffusion is the emitter. Notice that the aluminum source contact connects the N+ and p diffusions together effectively shorting the base emitter junction. Unfortunately, the p region will still have some resistance so that the parasitic BJT is not completely deactivated.

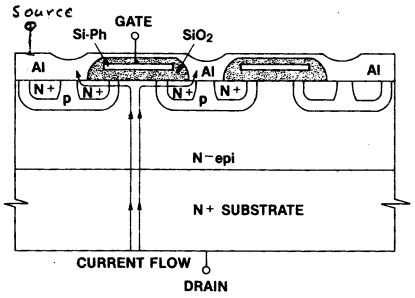

Figure 6

A more complete model for the power MOSFET including the gate resistance, interterminal capacitances and parasitic BJT is shown in Figure 7. In this type of device either the MOSFET or the BJT can be triggered on. The element which conducts first depends on the external gate to source resistance, R_{GS}. If R_{GS} is small (<1Ω) then it is the BJT that will trigger first. A typical 400V MOSFET

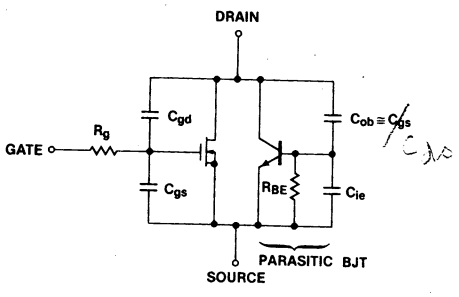

Figure 7

will have a dV/dt threshold of >75V/nsec which is more than adequate for most applications. In fact it is quite difficult to generate transitions that will produce false triggering in devices introduced since 1979. The earlier devices (1976-1978) are for the most part relatively small (V_{DS}=80,$R_{DS(ON)}$= 2.5Ω) and many of these can be turned on by transitions of 5 to 20 V/nsec.

dV/dt TEST CIRCUITS

If it is suspected that there may be a dV/dt problem in a particular design, the best course of action would be to measure the dV/dt capability of the switches being used. One possible circuit is given in Figure 8.

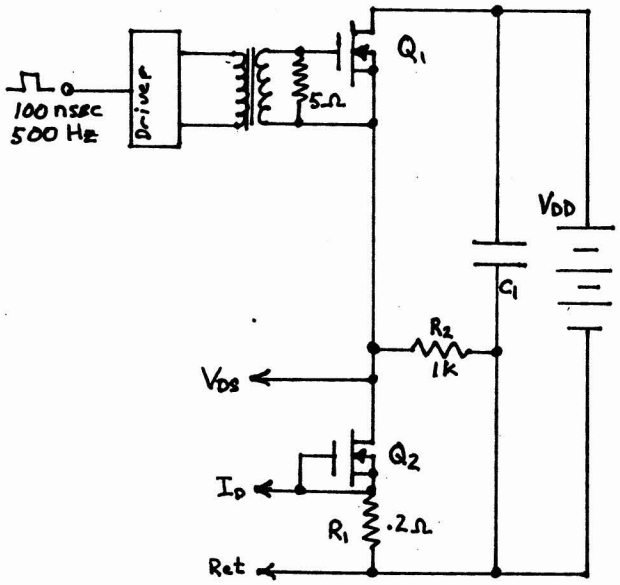

Figure 8

The device under test is Q_2. Q_1 is a very fast switch driven from a pulse generator through T_1. By driving the gate of Q_1 with a very fast pulse and an amplitude of 18 to 20V, Q_1 can be turned on in 5 nsec. From a 400V source this will provide a 80V/nsec transition across Q_2. The current through Q_2 is measured by looking at the voltage across R_1. R_1 is used for current viewing in preferance to a current probe for several reasons:

1. The upper frequency response of most probes is not adequate for the speeds present in this test circuit.

2. Most current probes will have delay times in excess of 10nsec. This makes it difficult to correlate the voltage and current waveforms properly in time.

3. The insertion of the current probe into the circuit will introduce an additional parasitic series inductance which will slow down the charging of C_{gs} and C_{gd} of Q_2. This is turn reduces the dV/dt of the transition from drain-to-source.

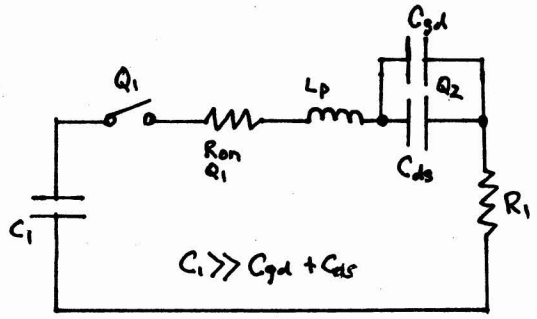

Figure 9 is an equivalent circuit. When Q_1 is turned on the current in the loop will ring as a damped sinusoid because the circuit is a series RLC. To achieve a rapid rise in voltage across Q_2, it is imperative that the parasitic inductance, L_p, be as small as possible.

Actual test waveforms for a power MOSFET are shown in Figures 10, 11 and 12 for an IVN5200 (.5Ω, 80V). In Figure 10 a 70V, 6 nsec transition is applied to Q_2. The current through Q_2 is, as predicted, a damped sinusoid, symetrical about zero. The transition voltage is next increased to 80V and, as shown in Figure 11, spurious triggering occurs. The current waveform is no longer a damped sinusoid. After an initial one cycle of ringing a DC current of approximately 1 A flows for 60nsec. This is due to triggering of the parasitic BJT.

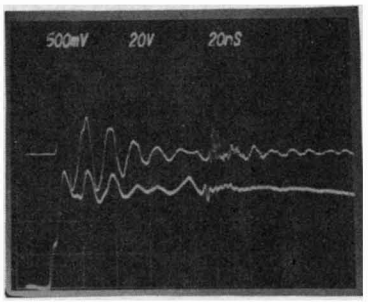

Figure 10

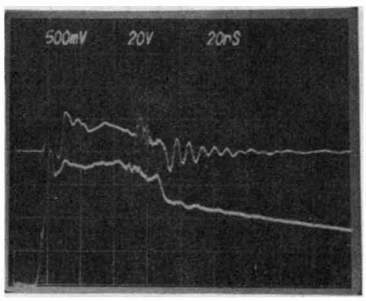

Figure 11

If V_{DD} is again reduced to 70V and 47Ω added in series with the gate of Q_2 then the voltage and current waveforms in Figure 12 will be seen. Q_2 is clearly being turned on and there is no hint of a series resonant circuit action. The impedance of Q_2 is so low that Q_1 cannot complete the rapid transition up to 70V. This is an example of triggering the MOSFET itself due to excessive gate to source impedance. In this particular device any resistance greater than 10Ω from gate to source would induce some triggering.

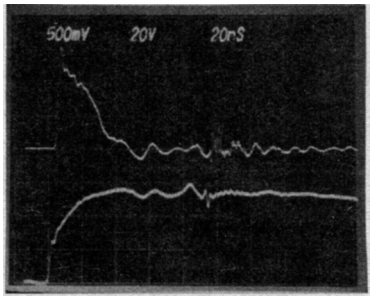

Figure 12

To examine the behavior of a device when reverse conduction is present, the test circuit in Figure 8 can be modified as shown in Figure 13 to include an inductor, L_1. A double pulse drive is now employed so that during the first pulse energy is stored in L_1. During the interpulse interval L_1 discharges through Q_2 in the reverse direction until the beginning of the second pulse. This allows the dV/dt capabilities to be measured when reverse conduction is present. Again the repitition rate is kept low to limit dissipation to a small value.

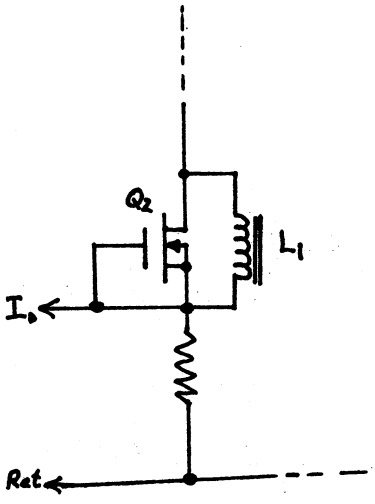

Figure 13

MEANS FOR REDUCING dV/dt TRIGGERING

There are a number of things that can be done to reduce dV/dt turn-on. The simplest and most obvious means would be to slow down the switching time. In the case of the power MOSFET a series resistance at the gate terminal can be used to produce any desired transition time. As was pointed out earlier however, any increase in the gate-to-source resistance decreases the dV/dt capability of the MOSFET proper. The addition of gate resistance will reduce the chances of turning on the parasitic bipolar but does nothing for the MOSFET itself unless the drive resistance is asymetrical, i.e. the resistance during the off state is smaller than during the on state. Figure 14 shows how this could be accomplished using a diode across the gate resistance.

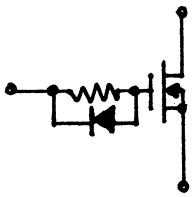

Figure 14

The collector-emitter or drain-source transition could also be slowed down by the use of a snubber network, either dissipative or with an energy recovery capability. Since such snubbers are frequently present in the circuit anyway only a change in component values might be needed.

The addition of capacitance from gate-to-source is another means to reduce dV/dt while increasing the immunity to turn-on.

The single most important means for limiting spurious turn-on is a low value for R_{GS} or R_{BE} during the off state.

Another possibility would be to apply a negative bias to the base or gate during the off state effectively requiring a large value for dV/dt in order to reach V_{th}.

If, however, there is a problem with reverse conduction then the foregoing methods may not be adequate. The most effective method in that case would be to eliminate the reverse conduction entirely by inserting a series diode in the collector or drain as shown in Figure 15. D_1 can be a low

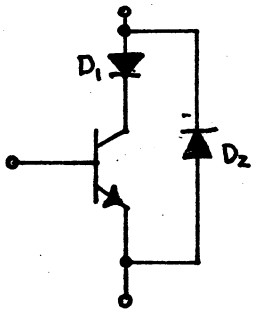

Figure 15

voltage Schottky diode to achieve low forward losses since the reverse voltage is limited to about one volt by D_2. D_2 must be rated to carry the full reverse current and have the same breakdown voltage as the switch.

It should be pointed out that BJT switches, using regenerative proportional base drive, are particularly susceptible to this type of false triggering. Even a slight degree of turn-on may be sufficient to trigger the drive circuit to turn-on the switch fully which will normally destroy the switch and may also destroy other switches in the circuit.

CONSLUSIONS

Spurious turn-on due to dV/dt triggering is a real possibility in high speed switching circuits. A simplified model has been examined which provides a first order explanation of the problem. Triggering of the parasitic BJT in the MOSFET is not a significant problem but triggering of the MOSFET itself or of a normal BJT is possible expecially if reverse condition is present in the switch. The designer however, has a number of means available to eliminate this problem in most circuits. What is most important is that the designer recognize the possibility of the problem and take steps to minimize it.

BIBLIOGRAPHY

(1) "The Power Transistor in its Environment", Thompson-CSF Semiconductor Division, Pages 165 to 180, October 1978.

(2) R. Severns, "Using the Power MOSFET as a Switch", Intersil Applications Note AO-36, January 1981.

APPENDIX 1

DERIVATION OF EQUIVALENT CIRCUIT TRANSIENT RESPONSE

For the purposes of calculating the voltage at the gate or base, the equivalent circuit shown in Figure 2 can be used with the appropriate component values. The ramp function is provided by the combination of a positive until ramp starting at t=0 and a negative unit ramp at $t=t_1$. The slope of the ramp, dV/dt, is:

$$\frac{dV}{dt} = \frac{E_1}{t_1} \qquad \text{(A1-1)}$$

The output voltage, $E_o(s)$, can be shown to be:

$$E_o(S) = \left(\frac{E_1}{t_1}\right)\left(\frac{C_1}{C_1+C_2}\right) \cdot \left[\frac{1}{S(S+1/R(C_1+C_2))} - \frac{e^{-t_1 s}}{S(S+1/R(C_1+C_2))}\right] \qquad \text{(A1-2)}$$

By applying the following inverse Laplace transformations to equation A1-2:

$$\frac{1}{S(S+\alpha))} \Longrightarrow \frac{1}{\alpha}\ (1-e^{-\alpha t}) \qquad \text{(A1-3)}$$

$$F(S)e^{-t_1 S} \Longrightarrow F(t-t_1) \qquad \text{(A1-4)}$$

The time domain response for $e_o(t)$ can be obtained as:

for: $t \leq t_1$

$$e_o(t) = \frac{E_1 RC_1}{t_1}\left\{1-e^{-t/R(C_1+C_2)}\right\} \qquad \text{(A1-5)}$$

and for $t \geq t_1$

$$e_o(t) = \frac{E_1}{t_1}(RC_1)\left\{e^{-t/R(C_1+C_2)}\right\} \cdot \left\{e^{t_1/R(C_1+C_2)}\right\} \qquad \text{(A1-6)}$$

The waveform represented by equations (A1-5) and (A1-6) was shown in Figure 3. For practical purposes, the only feature of the waveform that is of interest is the peak value of e_o. By combining equations (A1-1) and (A105) and setting $t=t_1$, the expression for e_{pk} becomes:

$$e_{pk} = \left(\frac{dV}{dt}\right)(\tau_1)\left(1-e^{-\frac{E_1}{dV/dt}}\right)\left(\frac{1}{\tau_2}\right) \qquad \text{(A1-7)}$$

where $\tau_1 = RC_1$ (A1-8)

$\tau_2 = R(C_1+C_2)$ (A1-9)

APPENDIX 2

POWER MOSFET SMALL SIGNAL CAPACITANCE MEASUREMENTS

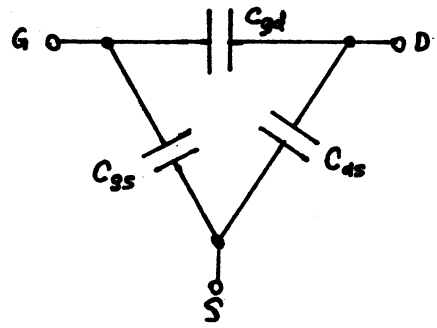

Figure A2-1

All of the capacitances are functions of V_{DS}.

Definitions

$$C_{iss} \equiv C_{gs} + C_{gd},\ C_{ds} = \text{short circuit}$$

$$C_{oss} \equiv C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs}+C_{gd}}$$

$$C_{oss} \simeq C_{ds} + C_{gd};\ C_{gs} = \text{short circuit}$$

$$C_{rss} \equiv C_{gd}$$

Measurement Techniques

The measurement is performed by shorting out one capacitance (C_{gs}, C_{gd} or C_{ds}) at a time and measuring the parallel capacitance of the remaining two with a 1Mhz capacitance bridge.

Three capacitances are measured:

$C_1 = C_{gs} + C_{gd}$

$C_2 = C_{gd} + C_{ds}$

$C_3 + C_{ds} + C_{gs}$

From the values of C_1, C_2 and C_3 the values for C_{iss}, C_{oss} and C_{rss} can be derived:

$$C_{iss} = C_1$$

$$C_{oss} \cong C_2$$

$$C_{rss} = \frac{C_1 + C_2 - C_3}{2}$$

Or if you prefer the values for C_{gd}, C_{gs} and C_{ds} may be calculated:

$$C_{gd} = \frac{C_1 + C_2 - C_3}{2}$$

$$C_{gs} = \frac{C_1 - C_2 + C_3}{2}$$

$$C_{ds} = \frac{-C_1 + C_2 + C_3}{2}$$

The actual test circuits are shown in Figure A2-7.

DERIVATION OF EQUATIONS

(1) $C_1 = C_{gs} + C_{gd}$

(2) $C_2 = C_{gd} + C_{ds}$

(3) $C_3 = C_{gs} + C_{ds}$

(1-2) $C_{gs} - C_{ds} + C_1 - C_2$

(3) $C_{gs} + C_{ds} = C_3$

$$C_{gs} = \frac{C_1 - C_2 + C_3}{2}$$

(2-1) $-C_{gs} + C_{ds} = -C_1 + C_2$

(3) $C_{gs} + C_{ds} = C_3$

$$C_{ds} = \frac{-C_1 + C_2 + C_3}{2}$$

(2-3) $C_{gd} - C_{gs} = C_2 - C_3$

(1) $C_{gd} + C_{gs} = C_1$

$$C_{gd} = \frac{C_1 + C_2 - C_3}{2}$$

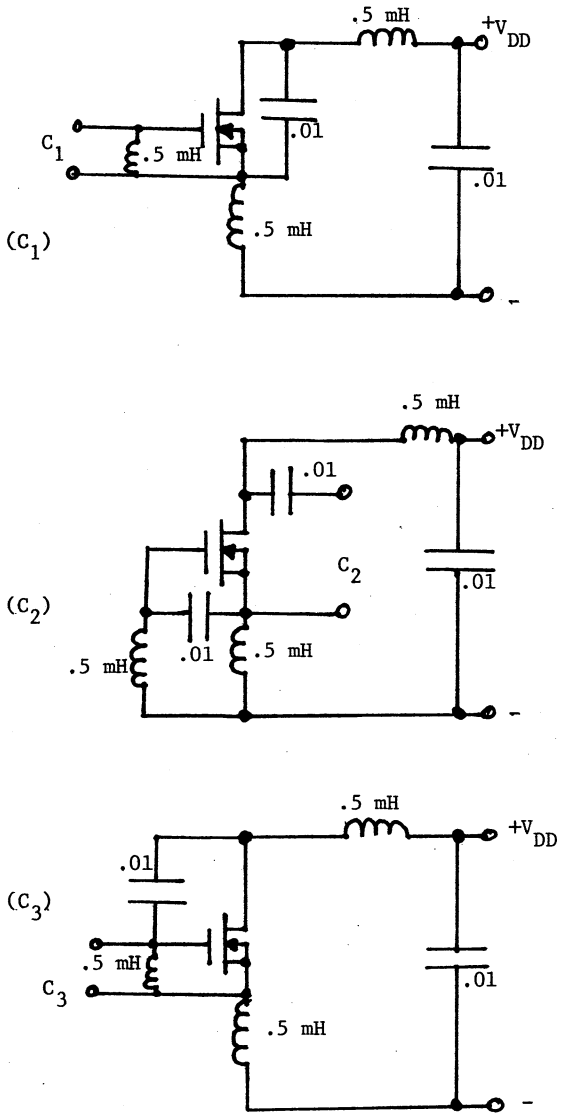

Figure A2-2